IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): The memory according to claim 27,~~A magnetic random access memory comprising:~~

~~a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format;~~

~~word lines respectively connected to rows of the memory cell array;~~

~~bit lines respectively connected to columns of the memory cell array;~~

~~a row decoder to select the word lines; and~~

~~a column decoder to select the bit lines,~~

wherein first electrical characteristic values based on storage data stored in a plurality of first memory cells are detected, the reference data is continuously written in the plurality of first memory cells, the reference data written in the plurality of first memory cells is continuously read out to detect second electrical characteristic values based on the reference data, and the first electrical characteristic values based on the storage data are compared with the second electrical characteristic values ~~those~~ based on the reference data to determine values of the storage data.

Claim 2 (Original): The memory according to claim 1, wherein a write/read of the reference data is executed in synchronism with an external clock.

Claim 3 (Original): The memory according to claim 1, wherein a write/read of the reference data is executed asynchronously to an external clock.

Claim 4 (Original): The memory according to claim 3, further comprising a column address buffer which is connected to the column decoder and receives a column address strobe signal, wherein the write/read of the reference data is executed while causing the column address buffer to receive each of a plurality of column addresses at each of continuous falling edges of the column address strobe signal.

Claim 5 (Original): The memory according to claim 3, further comprising a column address buffer which is connected to the column decoder, has a counter function, and receives a column address strobe signal, wherein the write/read of the reference data is executed while causing the counter function to increment a column address number from a column address designated first, at each of continuous falling edges of the column address strobe signal.

Claim 6 (Original): The memory according to claim 3, further comprising a column address buffer which is connected to the column decoder and receives a column address strobe signal, wherein the write/read of the reference data is executed while changing a column address to be sent to the column address buffer while keeping the column address strobe signal at low level.

Claim 7 (Original): The memory according to claim 1, further comprising a control section which generates an address signal to be supplied to the row decoder and the column decoder.

Claim 8 (Currently Amended): The memory according to claim 27,~~A magnetic random access memory comprising:~~

~~a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format;~~

~~word lines respectively connected to rows of the memory cell array;~~

~~bit lines respectively connected to columns of the memory cell array;~~

~~a row decoder to select the word lines; and~~

~~a column decoder to select the bit lines,~~

wherein a data write is set to continuously write data in a plurality of first arbitrary memory cells, and a data read is set to continuously read out storage data stored in a plurality of second arbitrary memory cells.

Claim 9 (Original): The memory according to claim 8, wherein a write/read of the reference data is executed in synchronism with an external clock.

Claim 10 (Original): The memory according to claim 8, wherein a write/read of the reference data is executed asynchronously to an external clock.

Claim 11 (Original): The memory according to claim 10, further comprising a column address buffer which is connected to the column decoder and receives a column address strobe signal, wherein the write/read of the reference data is executed while causing the column address buffer to receive each of a plurality of column addresses at each of continuous falling edges of the column address strobe signal.

Claim 12 (Original): The memory according to claim 10, further comprising a column address buffer which is connected to the column decoder, has a counter function, and

receives a column address strobe signal, wherein the write/read of the reference data is executed while causing the counter function to increment a column address number from a column address designated first, at each of continuous falling edges of the column address strobe signal.

Claim 13 (Original): The memory according to claim 10, further comprising a column address buffer which is connected to the column decoder and receives a column address strobe signal, wherein the write/read of the reference data is executed while changing a column address to be sent to the column address buffer while keeping the column address strobe signal at low level.

Claim 14 (Original): The memory according to claim 8, further comprising a control section which generates an address signal to be supplied to the row decoder and the column decoder.

Claim 15 (Canceled).

Claim 16 (Currently Amended): ~~The method according to claim 15,~~ A driving method of a magnetic random access memory which comprises:

a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format,

word lines respectively connected to rows of the memory cell array,

bit lines respectively connected to columns of the memory cell array,

a row decoder to select the word lines, and

a column decoder to select the bit lines,

the method comprising:

detecting electrical characteristic values based on storage data stored in a plurality of memory cells;

continuously writing reference data in the plurality of memory cells;

continuously reading out the reference data written in the plurality of memory cells to detect electrical characteristic values based on the reference data; and

comparing the electrical characteristic values based on the storage data with those based on the reference data to determine values of the storage data, wherein a write/read of the reference data is executed in synchronism with an external clock.

Claim 17 (Currently Amended): ~~The method according to claim 15,~~ A driving method of a magnetic random access memory which comprises:

a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format,

word lines respectively connected to rows of the memory cell array,

bit lines respectively connected to columns of the memory cell array,

a row decoder to select the word lines, and

a column decoder to select the bit lines,

the method comprising:

detecting electrical characteristic values based on storage data stored in a plurality of memory cells;

continuously writing reference data in the plurality of memory cells;

continuously reading out the reference data written in the plurality of memory cells to detect electrical characteristic values based on the reference data; and

comparing the electrical characteristic values based on the storage data with those based on the reference data to determine values of the storage data, wherein a write/read of the reference data is executed asynchronously to an external clock.

Claim 18 (Original): The method according to claim 17, wherein

the magnetic random access memory further comprises a column address buffer which is connected to the column decoder and receives a column address strobe signal, and

in the method, the write/read of the reference data is executed while causing the column address buffer to receive each of a plurality of column addresses at each of continuous falling edges of the column address strobe signal.

Claim 19 (Original): The method according to claim 17, wherein

the magnetic random access memory further comprises a column address buffer which is connected to the column decoder, has a counter function, and receives a column address strobe signal, and

in the method, the write/read of the reference data is executed while causing the counter function to increment a column address number from a column address designated first, at each of continuous falling edges of the column address strobe signal.

Claim 20 (Original): The method according to claim 17, wherein

the magnetic random access memory further comprises a column address buffer which is connected to the column decoder and receives a column address strobe signal, and

in the method, the write/read of the reference data is executed while changing a column address to be sent to the column address buffer while keeping the column address strobe signal at low level.

Claim 21 (Canceled).

Claim 22 (Currently Amended): ~~The method according to claim 21,~~ A driving method of a magnetic random access memory which comprises:

a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format,

word lines respectively connected to rows of the memory cell array,

bit lines respectively connected to columns of the memory cell array,

a row decoder to select the word lines, and

a column decoder to select the bit lines,

the method comprising:

executing a data write which is set to continuously write data in a plurality of first arbitrary memory cells; and

executing a data read which is set to continuously read out storage data stored in a plurality of second arbitrary memory cells, wherein a write/read of the reference data is executed in synchronism with an external clock.

Claim 23 (Currently Amended): ~~The method according to claim 21,~~ A driving method of a magnetic random access memory which comprises:

a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format,

word lines respectively connected to rows of the memory cell array,

bit lines respectively connected to columns of the memory cell array,

a row decoder to select the word lines, and

a column decoder to select the bit lines,

the method comprising:

executing a data write which is set to continuously write data in a plurality of first arbitrary memory cells; and

executing a data read which is set to continuously read out storage data stored in a plurality of second arbitrary memory cells, wherein a write/read of the reference data is executed asynchronously to an external clock.

Claim 24 (Original): The method according to claim 23, wherein

the magnetic random access memory further comprises a column address buffer which is connected to the column decoder and receives a column address strobe signal, and

in the method, the write/read of the reference data is executed while causing the column address buffer to receive each of a plurality of column addresses at each of continuous falling edges of the column address strobe signal.

Claim 25 (Original): The method according to claim 23, wherein

the magnetic random access memory further comprises a column address buffer which is connected to the column decoder, has a counter function, and receives a column address strobe signal, and

in the method, the write/read of the reference data is executed while causing the counter function to increase a column address number from a column address designated first, at each of continuous falling edges of the column address strobe signal.

Claim 26 (Original): The method according to claim 23, wherein

the magnetic random access memory further comprises a column address buffer which is connected to the column decoder and receives a column address strobe signal, and

in the method, the write/read of the reference data is executed while changing a column address to be sent to the column address buffer while keeping the column address strobe signal at low level.

Claim 27 (Original): A magnetic random access memory comprising:

a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format;

word lines respectively connected to rows of the memory cell array;

bit lines respectively connected to columns of the memory cell array;

a row decoder to select the word lines;

a column decoder to select the bit lines;

a first buffer to store detected electrical characteristic values based on storage data stored in a plurality of memory cells;

a second buffer to store continuously detected electrical characteristic values based on reference data written in the plurality of memory cells; and

a comparator to compare the electrical characteristic values based on the storage data with those based on the reference data to determine values of the storage data.

Claim 28 (Original): The memory according to claim 27, further comprising a column address buffer which is connected to the column decoder and receives a column address strobe signal.

Claim 29 (Original): The memory according to claim 28, the column address buffer has a counter function.

Claim 30 (Original): The memory according to claim 27, further comprising a control section which generates an address signal to be supplied to the row decoder and the column decoder.

Claim 31 (Canceled).

Claim 32 (Currently Amended): ~~The memory according to claim 31,~~ A magnetic random access memory comprising:

a memory cell array in which memory cells, each having a magnetoresistive element as a storage element, are arranged in correspondence with addresses that are arranged in a matrix format;

word lines respectively connected to rows of the memory cell array;

bit lines respectively connected to columns of the memory cell array;

a row decoder to select the word lines;

a column decoder to select the bit lines; and

a setting section to set a data write to continuously write data in a plurality of first arbitrary memory cells, and set a data read to continuously read out storage data stored in a

plurality of second arbitrary memory cells, further comprising a column address buffer which is connected to the column decoder and receives a column address strobe signal.

Claim 33 (Original): The memory according to claim 32, the column address buffer has a counter function.

Claim 34 (Currently Amended): The memory according to claim [[31]] 32, further comprising a control section which generates an address signal to be supplied to the row decoder and the column decoder.